REMARKS

The Final Office Action mailed on April 1, 2003, has been received and reviewed.

Claims 31-35 and 37-45 are currently pending in the above-referenced application. Each of claims 31-35 and 37-45 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 33, 34, 37-41, 44, and 45 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In particular, it each of claims 33, 34, 37-41, 44, and 45 has been rejected for reciting a structure which includes both hemispherical-grain (HSG) polysilicon on or over a storage poly and dielectric material lining recesses that have been formed in the storage poly. The Office has taken the position that the specification of the above-referenced application does not provide an adequate written description for the subject matter recited in claims 33, 34, 37-41, 44, and 45.

It is respectfully submitted that the specification of the above-referenced application does provide an adequate written description for the subject matter recited in each of claims 33, 34, 37-41, 44, and 45. M.P.E.P. § 2163.02 provides that the "subject matter of the claim need not be described literally (i.e., using the same terms in *in haec verba*) for the disclosure to satisfy the written description requirement. While the specification of the above-referenced application does not expressly state whether or not the HSG polysilicon is left on or removed from the polysilicon layer over which it is formed use of the HSG polysilicon to pattern the polysilicon layer, it is respectfully submitted that it would be clear to one of ordinary skill in the art that the polysilicon could be left in place following patterning and prior to the introduction of a dielectric or insulative coating into recesses that have been formed in the polysilicon layer. Notably, it would not matter if the HSG polysilicon remained in place, as it may have the same electrical conductivity properties as the remaining portions of the underlying polysilicon layer. This is one of the reasons why, following the patterning of the underlying polysilicon layer, the HSG

polysilicon does not appear as a separate element. To many of skill in the art, the extra process steps that would be required to remove the HSG polysilicon and clean the structure would be undesirable, as extra process steps increase the likelihood of damage to a device under fabrication and, thus, the probability of device failure.

Of course, this does not exclude the possibility that the HSG polysilicon could also be removed from the remaining portions of the underlying, patterned layer of polysilicon.

Accordingly, it is respectfully submitted that the specification provides an adequate written description of the subject matter recited in claims 33, 34, 37-41, 44, and 45. Therefore, withdrawal of the 35 U.S.C. § 112, first paragraph, rejections of claims 33, 34, 37-41, 44, and 45 is respectfully requested.

Rejections Under 35 U.S.C. § 102(b)

Each of claims 31-35 and 37-45 stands rejected under 35 U.S.C. § 102(b).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Woo

Claims 31-35 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,405,799 to Woo et al. (hereinafter "Woo").

Woo describes a structure that, as depicted in FIG. 2 thereof, includes a bottom conductive plate 16, conductive bars 23 thereon, and an upper conductive plate 25 over the bars 23, with the bars 23 electrically connecting the bottom conductive plate 16 and the upper conductive plate 25. At col. 4, lines 9-14, and in FIG. 10, Woo describes and illustrates the bars 23 as comprising polysilicon layers 18 that "remain as islands of various shapes" which overlie remaining portions of an insulating layer 17, which portions are also referred to in Woo

as an insulating layer pattern 19. *See* FIGs. 5 and 6; col. 3, lines 27-38. Thereafter, a conductive layer 20 is deposited over and between the insulating layer pattern 19. FIG. 7; col. 3, lines 39-48.

Independent claim 31 recites a semiconductor storage capacitor poly that includes downwardly extending recesses and a plurality of contiguous mesas that comprise a plurality of contiguous top surfaces forming a maze-like structure.

The polysilicon layer 18 of Woo is not a storage poly. Rather, as FIGs. 4-7 and col. 3, lines 10-48 of Woo clearly indicate, the polysilicon layer 18 merely acts as a mask which is used to form an insulating layer pattern 19 from an underlying insulating layer 17. Thus, it is respectfully submitted that Woo does not expressly or inherently describe a storage poly that includes a plurality of mesas but, rather, an insulating layer pattern 19 that includes a plurality of mesas.

Moreover, as the islands of the insulating layer pattern 19 of Woo are formed prior to deposition of conductive material around the islands to form a conductive layer 20, the resulting structure, if it could be properly referred to as a "storage poly," does not include downwardly extending recesses, as recited in independent claim 31.

Further, the term "contiguous" is defined by Merriam-Webster's Collegiate Dictionary, Tenth Edition, as "being in actual contact : touching along a boundary or at a point. . . . touching or connected throughout in an unbroken sequence . . ." As used in independent claim 33, it is clear that the webs themselves must be connected to one another, and that the top surfaces of the webs must be connected to one another.

By way of contrast, Woo lacks any express or inherent description of a capacitor storage poly that includes a plurality of contiguous webs that comprise a plurality of contiguous top surfaces that form a maze-like structure. Instead of contiguous webs, the description of Woo is limited to a polysilicon layer 18 which includes "as *islands* of various shapes." (Emphasis supplied). As the term "islands" refers to structures which are discrete from one another (Merriam-Webster's Collegiate Dictionary, Tenth Edition, defines "island" as "an isolated group or area . . ."), and since Woo does not describe that the islands of polysilicon layer 18 may be connected to one another, it is clear that neither the islands of polysilicon layer 18 nor their top surfaces are contiguous.

Also, the Tenth Edition of Merriam-Webster's Collegiate Dictionary defines "maze" as "a confusing intricate network of passages."

Since Woo describes the polysilicon layers 18 as remaining "as *islands* of various shapes" (emphasis supplied), and depicts the passageways around these islands, which passageways are illustrated in FIG. 10 as insulating layer 17, as completely surrounding the islands of polysilicon layer 18 and, thus, as being neither confusing nor intricate. It is, therefore, respectfully submitted that Woo neither expressly nor inherently describes that the polysilicon layer 18 thereof comprises "a plurality of contiguous mesas" or that form "a maze-like structure."

Thus, under 35 U.S.C. § 102(b), independent claim 31 is allowable over Woo.

Claim 32 is allowable, among other reasons, as depending from claim 31, which is allowable.

Independent claim 33 also recites a semiconductor capacitor storage poly. The capacitor storage poly of independent claim 33 includes downwardly extending recesses, a plurality of contiguous webs that comprise contiguous top surfaces, and hemispherical-grain polysilicon on at least some of the contiguous top surfaces.

Again, the polysilicon layer 18 of Woo is not a storage poly—it is a mask which is used to form an insulating layer pattern 19 that is to be subsequently used to define a storage poly (conductive layer 20).

Furthermore, Woo includes no express or inherent description of a storage poly structure that includes downwardly extending recesses. Rather, the conductive layer 20 if Woo, which is the only feature thereof that could be reasonably referred to as a "storage poly," is formed after an insulating layer pattern 19 has already been formed. Thus, the structures that are described in Woo could not include any recesses that extend downwardly into the conductive layer 20.

Moreover, Woo lacks any express or inherent description of a capacitor storage poly that includes a plurality of contiguous webs that comprise a plurality of contiguous top surfaces. Instead of contiguous webs, the description of Woo is limited to a polysilicon layer 18 which includes "as *islands* of various shapes." (Emphasis supplied). As the term "islands" refers to structures which are discrete from one another (Merriam-Webster's Collegiate Dictionary, Tenth

Edition, defines "island" as "an isolated group or area . . ."), and since Woo does not describe that the islands of polysilicon layer 18 may be connected to one another, it is clear that neither the islands of polysilicon layer 18 nor their top surfaces are contiguous. Therefore, it is respectfully submitted that Woo does not anticipate each and every element of independent claim 33.

Accordingly, under 35 U.S.C. § 102(b), independent claim 33 is allowable over Woo.

Claim 34 is allowable, among other reasons, as depending from claim 33, which is allowable.

Independent claim 35 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a contiguous hemispherical-grain polysilicon layer on and in contact with the storage poly structure, and a mask over the hemispherical-grain polysilicon layer. Recesses in the storage poly structure are exposed through the contiguous hemispherical-grain polysilicon layer and the mask.

As Woo describes that the islands of the polysilicon layer 18 depicted in FIG. 10 are located over remaining portions of a second insulating layer 17, or an insulating layer pattern 19, they cannot be on an in contact with a storage poly structure, as recited in independent claim 35.

Furthermore, Woo neither expressly nor inherently describes a storage poly structure with downwardly extending recesses. Again, the description of Woo is limited to an insulating layer pattern 19 with downwardly extending recesses, which recesses are to be subsequently filled with portions of a conductive layer 20, which would comprise the storage poly structure.

In addition, Woo does not expressly or inherently describe a hemispherical-grain polysilicon layer that is on and in contact with a storage poly structure. Rather, the description of Woo is limited to a polysilicon layer 18 that overlies and contacts an insulating layer 17 that is on a bottom conductive plate 16. *See* FIGs. 4 and 5; col. 3, lines 10-33.

Further, as explained above, the islands of the polysilicon layer 18, which are, by definition, separate, cannot be contiguous with one another.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 35 is allowable over Woo.

Kenney

Claims 35 and 37-45 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,254,503 to Kenney (hereinafter "Kenney").

Kenney describes storage poly structures and methods for fabricating such structures. In particular, Kenney discloses two methods for forming high surface area storage poly structures, as well as two corresponding intermediate structures.

One intermediate structure of Kenney, shown in FIG. 4 thereof, includes recesses 20 that are formed at areas that are located beneath regions where the high points of surface irregularities 14, such as hemispherical-grain polysilicon, previously resided. It appears from FIG. 4 that the surface irregularities 14 may have been formed directly on the storage poly structure.

The other intermediate structure, which is depicted in FIG. 5 of Kenney, includes surface irregularities 14, such as hemispherical-grain polysilicon, which are formed on a layer 12 of silicon dioxide that, in turn, is formed over the storage poly structure. Col. 4, lines 50-55. Recesses 21 in the silicon dioxide layer 12 and, thus, in the storage poly structure are formed beneath locations where low-elevation regions of the surface irregularities 14 previously resided.

Independent claim 35 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a contiguous hemispherical-grain polysilicon layer on and in contact with the storage poly structure, and a mask over the hemispherical-grain polysilicon layer. Recesses in the storage poly structure are exposed through the contiguous hemispherical-grain polysilicon layer and the mask.

Kenney neither expressly or inherently describes that either the structure shown in FIG. 4 thereof or the structure shown in FIG. 5 thereof includes a contiguous layer of hemispherical-grain polysilicon. Instead, Kenney lacks any express or inherent description that both the surface irregularities 14 and the underlying region 12 of a substrate 10 may both be are formed from hemispherical-grain polysilicon. Further, FIGs. 1-4 depict the surface irregularities 14, which may comprise hemispherical-grain polysilicon, as being spaced apart from one another, not as being contiguous with one another.

The structure shown in FIG. 5 of Kenney does not include a contiguous layer of hemispherical-grain polyslicon on and in contact with a storage poly structure *and* a mask over

the hemispherical-grain polysilicon layer. More specifically, Kenney lacks any express or inherent description that the structure shown in FIG. 5 thereof ever requires or includes a mask. Moreover, Kenney lacks any express or inherent description that the structure shown in FIG. 5 includes a contiguous layer of hemispherical-grain polysilicon. Instead, if hemispherical-grain polysilicon were used, lower-elevation regions thereof would have been removed to form recesses, with only the spaced-apart (*i.e.,* not contiguous), upper regions of the hemispherical-grain polysilicon remaining. Further, the layer of hemispherical-grain polysilicon shown in FIG. 5 is not in contact with the storage poly structure but, rather, with an intervening layer 12 of silicon dioxide. Col. 4, lines 50-55.

For these reasons, it is respectfully submitted that Kenney does not expressly or inherently describe an embodiment which anticipates each and every element of independent claim 35. Thus, under 35 U.S.C. § 102(b), independent claim 35 is allowable over Kenney.

Independent claim 37 recites an intermediate semiconductor memory cell structure that includes a storage poly structure, a plurality of contiguous low elevation regions of a hemispherical-grain polysilicon layer on and in contact with the storage poly structure, recesses formed in the storage poly structure laterally between the low elevation regions, and dielectric material at least lining the recesses.

In FIGs. 1-4 of Kenney, the low-elevation regions of the surface irregularities 14, which may or may not comprise hemispherical-grain polysilicon, are shown as being spaced apart from one another, not as being contiguous with each other. As Kenney lacks any express or inherent description of a structure that includes a plurality of contiguous low elevation regions of a hemispherical-grain polysilicon layer, it is respectfully submitted that Kenney does not anticipate each and every element of independent claim 37.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 37 is allowable over Kenney.

Independent claim 38 recites a semiconductor memory cell structure that includes "regions of hemispherical-grain polysilicon on at least portions of an upper surface of said

storage poly structure . . . and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses".

Kenney does not include any express or inherent description of a semiconductor memory cell structure that includes hemispherical-grain polysilicon on the top surfaces of a storage poly structure, the recesses of which are substantially coated with a dielectric layer. To the contrary, at col. 4, lines 38-40, Kenney provides for removal of the "mask forming layers" from at least the structure shown in FIG. 4, which "mask forming layers" appear to include both the surface irregularities 14 and the masking layer 16, prior to the formation of a dielectric coating within recesses of the resulting storage poly structure.

With respect to the description that accompanies FIG. 5 of Kenney, it is clear that if hemispherical-grain polysilicon were used to form the surface irregularities 14, that the hemispherical-grain polysilicon would not be located on a storage poly structure but, rather, on a layer 12 of silicon dioxide that, in turn, has been placed on the storage poly structure. Col. 4, lines 50-55.

For these reasons, it is respectfully submitted that Kenney does not anticipate each and every element of independent claim 38 and, thus, that, under 35 U.S.C. § 102(b), independent claim 38 is allowable over Kenney.

Claims 39-41 are each allowable, among other reasons, as depending from claim 38, which is allowable.

Independent claim 42 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a substantially confluent hemispherical-grain polysilicon layer on the storage poly structure, and a mask positioned over the hemispherical-grain polysilicon layer. Elevated portions of the hemispherical-grain polysilicon layer are exposed through the mask.

Kenney lacks any express or inherent description of an intermediate structure that includes a substantially confluent layer of hemispherical-grain polysilicon. In particular, Kenney illustrates that the surface irregularities 14 are isolated from one another, meaning that they are not substantially confluent (*i.e.,* flow or come together; *see* Merriam-Webster's Collegiate

Dictionary, Tenth Edition). Further, Kenney lacks any express or inherent description that both the surface irregularities 14 and the underlying region 12 of a substrate 10 may both be formed from hemispherical-grain polysilicon, which is the only other way that Kenney could inclue a substantially confluent hemispherical-grain polysilicon layer, as required by independent claim 42.

Therefore, Kenney does not anticipate each and every element of independent claim 42. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 42 is allowable over Kenney.

Independent claim 43 also recites an intermediate semiconductor capacitor structure. The intermediate semiconductor capacitor structure of independent claim 43 includes a storage poly structure with recesses therein, remaining portions of a hemispherical-grain polysilicon layer substantially overlying upper portions of the storage poly structure, and a mask positioned over the hemispherical-grain polysilicon layer. The mask is located laterally between the recesses in the storage poly structure, with the recesses being exposed therethrough, and is substantially spaced apart from the storage poly structure by way of the remaining portions of hemispherical-grain polysilicon layer.

Kenney neither expressly nor inherently describes an intermediate semiconductor capacitor structure that includes portions of a hemispherical-grain polysilicon layer that substantially overlie upper portions the storage poly structure or that the mask thereof is substantially spaced apart from storage poly structure by way of the remaining portions of the hemispherical-grain polysilicon layer described therein. Instead, FIGs. 2-4 of Kenney, which are the only figures in Kenney that illustrate a mask 16, quite clearly depicts the mask 16 as contacting the upper surface of item 12, which is apparently a storage poly structure.

Therefore, it is respectfully submitted that Kenney does not anticipate each and every element of independent claim 43 and, thus, that, under 35 U.S.C. § 102(b), independent claim 43 is allowable over Kenney.

Independent claim 44 recites an intermediate semiconductor capacitor structure that includes a storage poly structure with recesses therein, a hemispherical-grain polysilicon layer on at least portions of the storage poly structure, and dielectric material lining at least the recesses.

Again, Kenney lacks any express or inherent description of an intermediate semiconductor capacitor structure which includes both dielectric material lining the recesses that are formed in a storage poly structure and hemispherical-grain polysilicon on portions of the storage poly structure.

Therefore, under 35 U.S.C. § 102(b), independent claim 44 is allowable over Kenney.

Independent claim 45 is directed to an intermediate semiconductor memory cell structure that includes a storage poly with recesses therein, low elevation regions of a hemispherical-grain polysilicon layer substantially covering an upper surface of the storage poly structure, and dielectric material at least lining the recesses.

Kenney neither expressly nor inherently describes an intermediate semiconductor capacitor structure which includes both dielectric material lining the recesses that are formed in a storage poly structure and hemispherical-grain polysilicon that substantially covers an upper surface of the storage poly structure.

Accordingly, under 35 U.S.C. § 102(b), independent claim 45 is allowable over Kenney.

Ahn

Claim 42 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,358,888 to Ahn et al. (hereinafter "Ahn").

Ahn teaches a method for manufacturing a capacitor and the structures that result from that method. Among other things, Ahn teaches, at col. 6, lines 31-48, forming HSG polysilicon grains that are "slightly separated from one another, thereby being formed as a group of islands."

Independent claim 42 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a substantially confluent hemispherical-grain polysilicon layer on the storage poly structure, and a mask positioned over the hemispherical-grain polysilicon

layer. Elevated portions of the hemispherical-grain polysilicon layer are exposed through the mask.

As "confluent" means "flowing or coming together" (Merriam-Webster's Collegiate Dictionary, Tenth Edition), and Ahn teaches that the hemispherical-grain polysilicon layer thereof includes islands that are separated, or isolated, from one another, Ahn does not expressly or inherently describe a structure which includes a substantially confluent hemispherical-grain polysilicon layer; *i.e.,* that the grains thereof flow or come together.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 42 is allowable over Ahn.

For the foregoing reasons, it is respectfully requested that the 35 U.S.C. § 102(b) rejections of claims 31-35 and 37-45 be withdrawn.

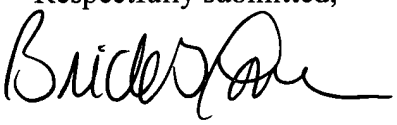
ENTRY OF AMENDMENT

It is respectfully requested that the amendment to the title presented herein be entered. It is submitted that the proposed amendment does not introduce new matter into the above-referenced application and would not require a new search. If the proposed amendment is not entered, entry thereof upon filing of a Notice of Appeal in the above-referenced application is respectfully requested.

CONCLUSION

It is respectfully submitted that each of claims 31-35 and 37-45 is allowable. An early indication of the allowability of each of these claims, and an indication that the above-referenced application has been passed for issuance, are respectfully solicited. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



Brick G. Power
Registration No. 38,581
Attorney for Applicant(s)
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: June 2, 2003

BGP/ps:djp
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